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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/774,890	02/09/2004	Eugene A. Fitzgerald	ASC-049C1	8754

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EXAMINER	
TRAN, MAI HUONG C	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/774,890	FITZGERALD, EUGENE A.	
	Examiner	Art Unit	
	Mai-Huong Tran	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

In the form PTO-1449 filed on 2/8/05, sheets 2 of 4, 3 of 4 and 4 of 4 have a different serial number, a different docket number, and a different applicant's name. They do not match to the application No. 10,774,890. Please submit the correct pages.

Claim Rejections - 35 U.S.C. § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3-5, 12, 19-22, 29-31 are rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent No. 6,690,043 to Usuda et al.

Regarding to claim 1, Usuda discloses a surface channel MOSFET comprising a relaxed planarized SiGe layer 31 on a substrate 1; a regrown Si.sub.1-xGe.sub.x layer 11 with thickness h; a Si channel layer 10; a gate dielectric 101; a polycrystalline semiconductor layer (col. 8, lines 49-50); and a highly conductive gate layer 102 (col. 13, lines 55-67, col. 14, lines 1-7, figs. 10A-10C, 11A-11C, and 12).

Regarding to claim 3, the MOSFET wherein the substrate comprises relaxed graded composition SiGe layers on Si (figs. 10A-10C, 11A-11C, and 12).

Regarding to claims 4, 30, the MOSFET wherein the substrate comprises Si (col. 13, line 25-29).

Regarding to claims 5, 31, the MOSFET wherein the substrate comprises Si with a layer of SiO.sub.2 (col. 13, lines 14-25, fig. 10C).

Regarding to claim 12, Usuda discloses a buried channel MOSFET comprising a relaxed planarized SiGe layer 31 on a substrate; a regrown Si.sub.1-xGe.sub.x layer 11 with thickness h; a Si channel layer 10; a Si.sub.1-yGe.sub.y layer 13; a second Si layer 1; a gate dielectric 101; a polycrystalline semiconductor layer (col. 8, lines 49-50); and a highly conductive gate metal layer 102 (col. 13, lines 55-67, col. 14, lines 1-7, figs. 10A-10C, 11A-11C, and 12).

Regarding to claims 19, 29, the MOSFET, wherein the substrate comprises relaxed graded composition SiGe layers on Si (col. 10, lines 25-33).

Regarding to claim 20, the MOSFET, wherein the substrate comprises Si (col. 10, line 25).

Regarding to claim 21, the MOSFET wherein the substrate comprises Si with a layer of SiO.sub.2 (col. 10, lines 25-28).

Regarding to claim 22, Usuda discloses a buried channel FET comprising a relaxed planarized SiGe layer 31 on a substrate; a regrown Si.sub.1-xGe.sub.x layer 11 with thickness h; a Si channel layer 10; a Si.sub.1-yGe.sub.y layer 13; a second Si layer 1; and a highly conductive gate layer 102 (col. 13, lines 55-67, col. 14, lines 1-7, figs. 10A-10C, 11A-11C, and 12).

Claim Rejections - 35 U.S.C. § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2, 6-11, 13-17, and 23-28 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,690,043 to Usuda et al. in view of the remark.

Regarding to claims 2, 7, 8, 13, 23 Usuda discloses the claimed invention except for the MOSFET wherein h is approximately 0.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form h is approximately 0, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding to claim 6, Usuda discloses the claimed invention except for a Ge channel layer.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form a Ge channel layer, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding to claims 8, 14, 24 Usuda discloses the claimed invention except for the MOSFET wherein the thickness of the Si layer is less than 5 nm.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the thickness of the Si layer is less than 5 nm, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding to claim 9, the MOSFET wherein the substrate comprises relaxed graded composition SiGe layers on Si (col. 10, lines 25-32).

Regarding to claim 10, the MOSFET, wherein the substrate comprises Si (col. 10, lines 25-35).

Regarding to claim 11, the MOSFET wherein the substrate comprises Si with a layer of SiO.sub.2 (col. 10, lines 25-35).

Regarding to claims 15, 25, the MOSFET wherein supply layer dopants are located in the Si.sub.1-yGe.sub.y layer (col. 8, lines 51-59).

Regarding to claims 16, 18, 26, 28, the MOSFET, wherein the supply layer dopants are implanted (col. 8, lines 51-59).

Regarding to claims 17, 27, the MOSFET, wherein the supply layer dopants are located below the Si channel layer (col. 8, lines 51-59).

Conclusion

Any inquiry concerning this communication on earlier communications from the examiner should be directed to Mai-Huong Tran, (571) 272-1796. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 6:30 PM. The examiner's supervisor, David Nelms can be reached on (571) 272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR, Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MH

Mai-Huong Tran